**Executive Summary**

For the first part of the assignment, a 4-bit comparator circuit was designed and tested on the DE1-SoC board with LEDs as outputs and sliding switches as inputs. Then, sequential assignment statements were used to design storage elements. Counters, clock divider, JK Flip Flop and a wrapper. A template of the testbench file was attained from Quartus and replaced the always part in order to run through all the possible cases. The code is then tested on Modelsim.

**Questions**

**Explain sVHDL code**

**Comparator:**

If Then structure is used in this part to divide different scenarios. The first scenario that needs to be consider is when (B + 1) overflows. When B is “1111”, other operations cannot proceed. So, the first case that is being handled is when B is “1111”, overflow is set to ‘1’ while other output remains the same. The rest of the three scenarios will be when A is greater than (B+1), when A is less than (B+1) and when A is equal to (B+1). The order of placement of these three scenarios does not matter. The code writing of these scenarios follow the rule in which wanted output are set to be ‘1’ and the rest of the output are set to be ‘0’s.

**JKFF:**

If Then clause is again used in this part of the code. A signal TMP is used to avoid having to let output Q act as input, which is also not allowed in VHDL. TMP is replacing Q in all the operations and Q is renewed to TMP’s state after operation. A nested If Then is used to make sure that all the operation happens when clock is at its rising edge. According to the truth table/behavior of the JKFF, when J = K = 0, Q do not change (same as the previous state). When J = K = 1, Q is opposite to its previous state. When J and K are different, Q follows the behavior of J. The above-mentioned scenarios are represented as conditions of the If Then clause in the JKFF VHDL code.

**Counter:**

A counter is by its name something that counts from (0)10 to (7)10. In binary it is represented by three bits, “000” to “111”. A signal tmp is used to avoid having to let output count act as input. An outer If Then clause is used to make sure that all other operations happen when the clock is at its rising edge. Then, the first nested If Then clause is used to describe the reset variable. When reset is ‘1’ then tmp is set to “000” to restart the counting. A second nested loop is used to do the count and reset to “000” when reach to “111”.

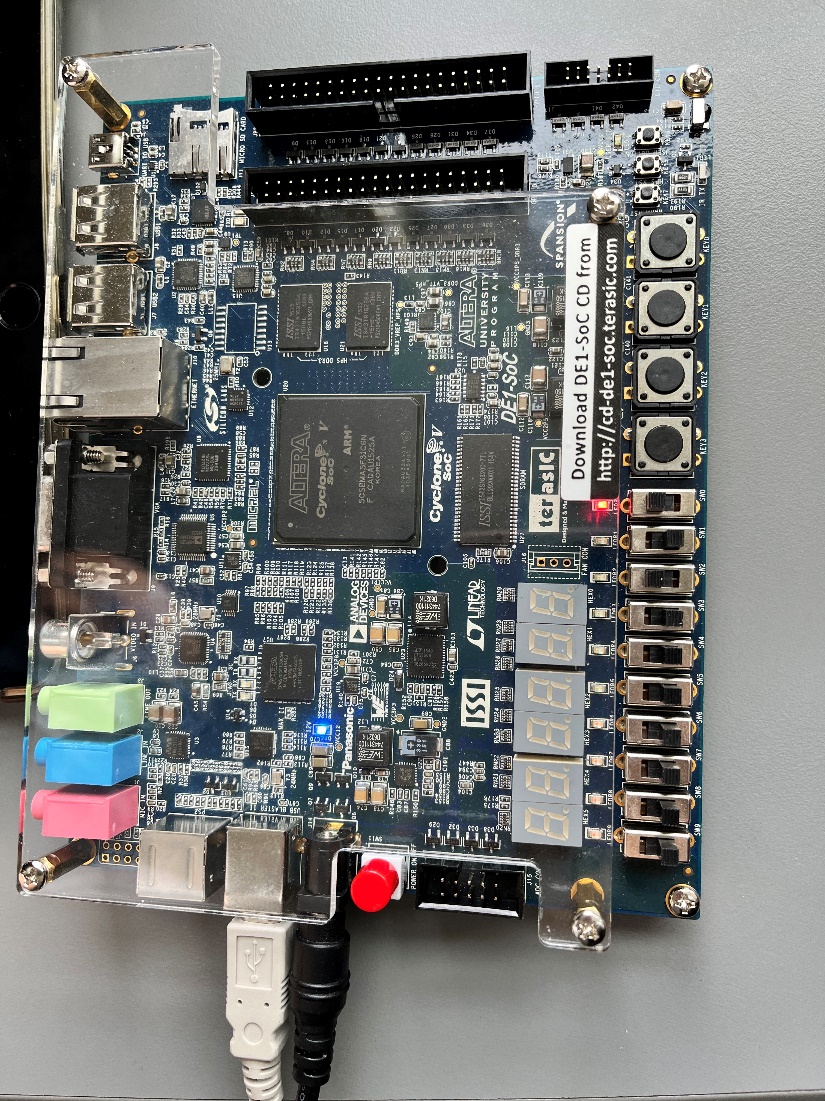
**Clock divider:**

The clock divider has a very similar structure as the counter, except it counts down from “111” to “000”. Also, its output is not count but the result of a NOR gate of the three bits of count. There is no count variable given in clock divider, thus, signal tmp is created as a three-bit vector to replace the function of count in Counter.

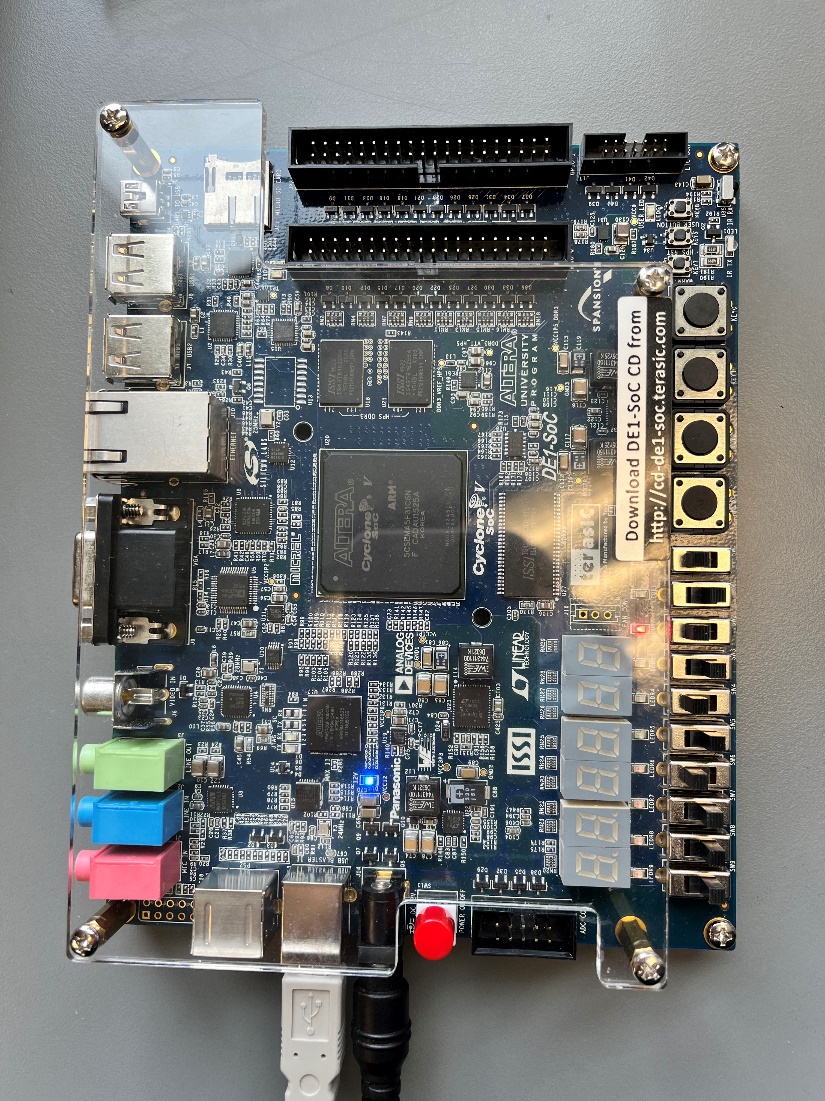
**Wrapper:**

Wrapper is simply a combined implication of clock divider, counter, and seven segment decoders. Three stages are used to connect clock divider to counter, counter to seven segment decoder and seven segment decoders to output. It is worth mentioning that the input of seven segment decoders is seven\_in which is a concatenation of ‘0’ and out\_c. Concatenation of ‘0’ is allowed because the counter only counts to decimal 7 which is 0111 in binary instead of 8 or 9.

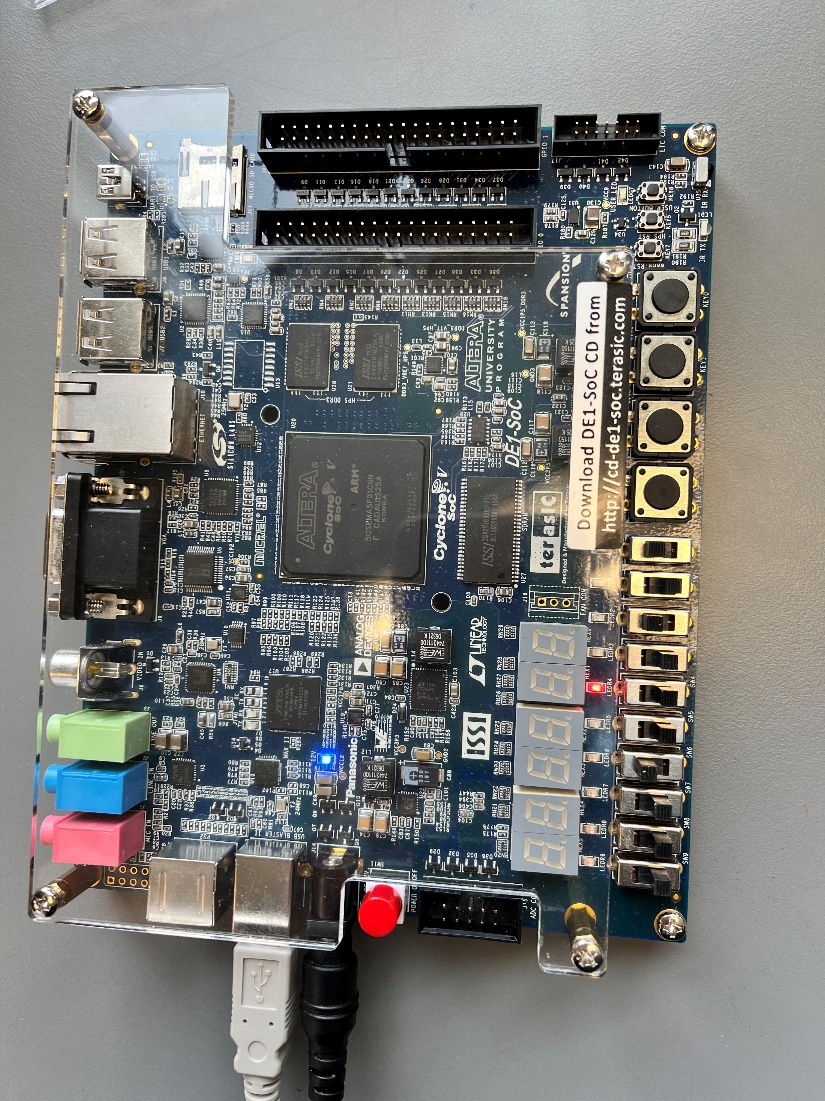
2. 4 plots from comparator



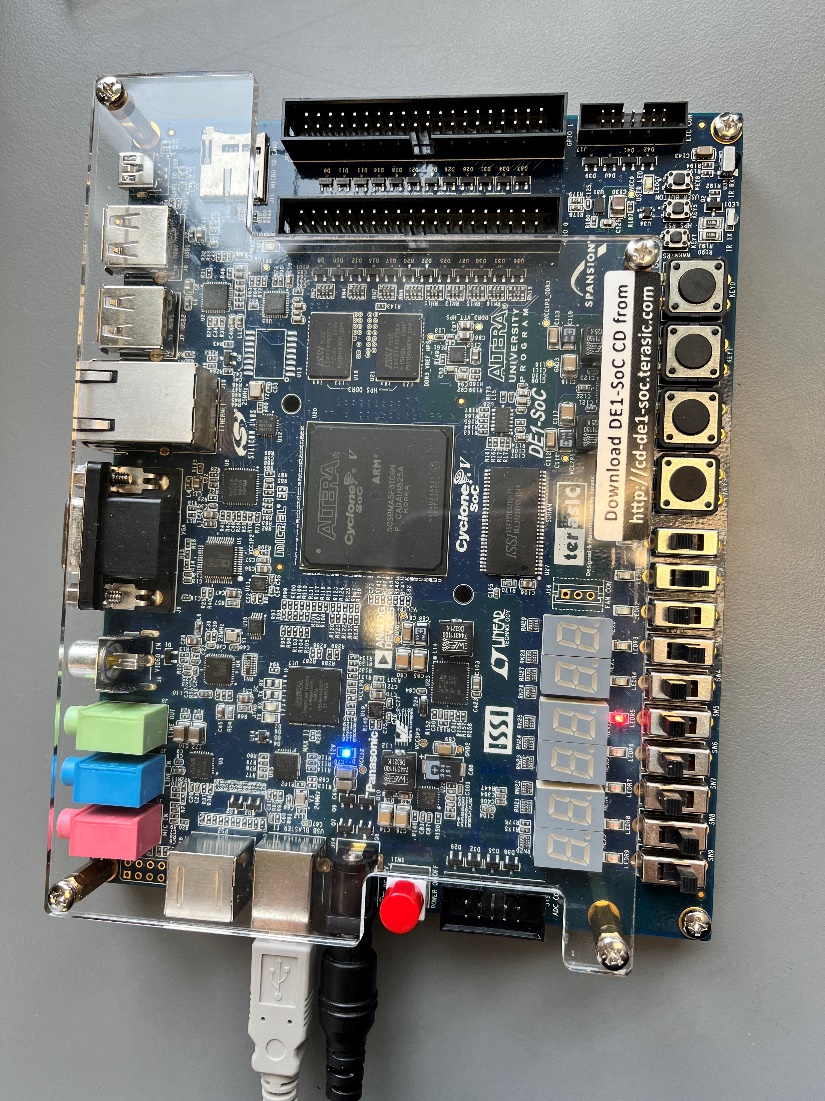
Above A >(B+1)



Above: A< (B+1)

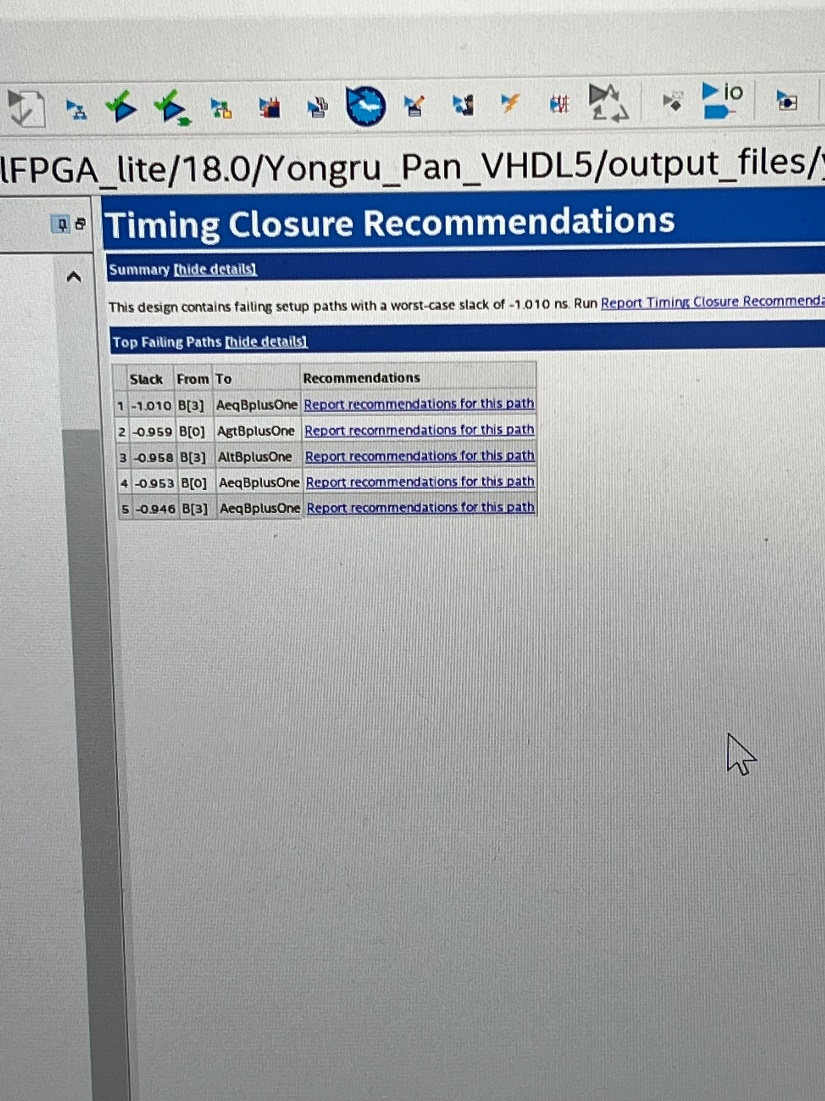


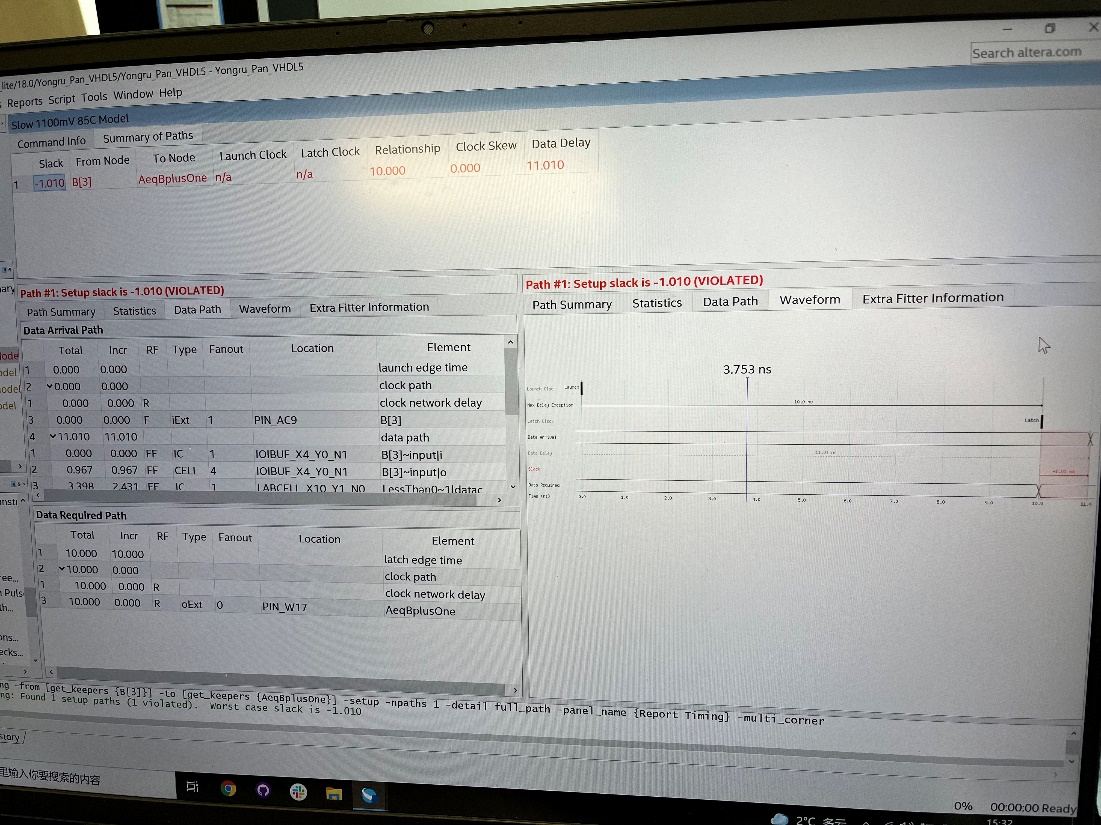
A = (B+1)



overflow

3. Critical path of comparator

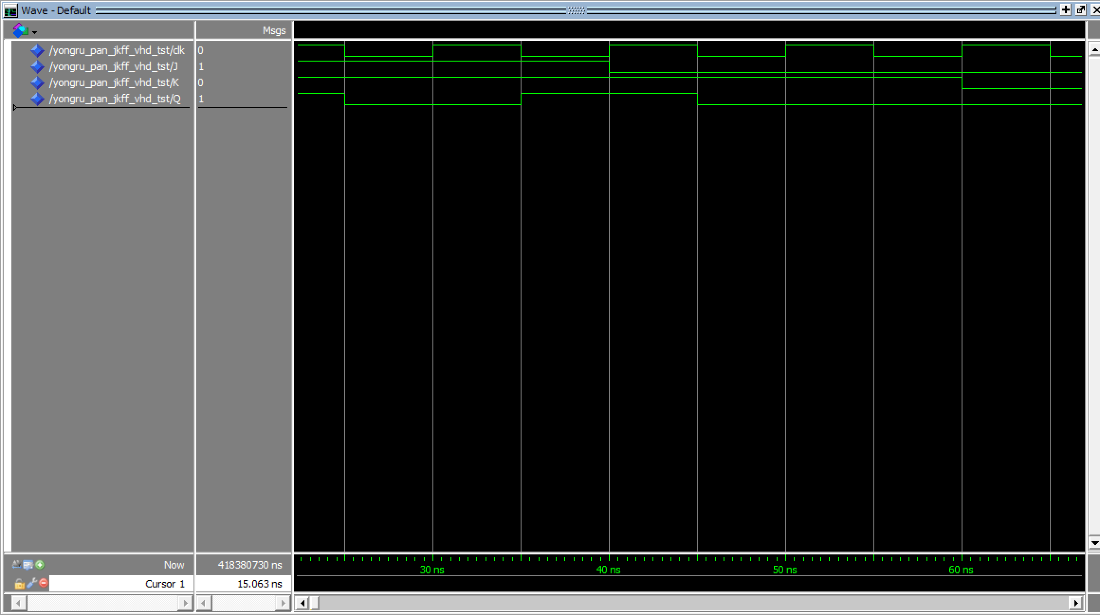




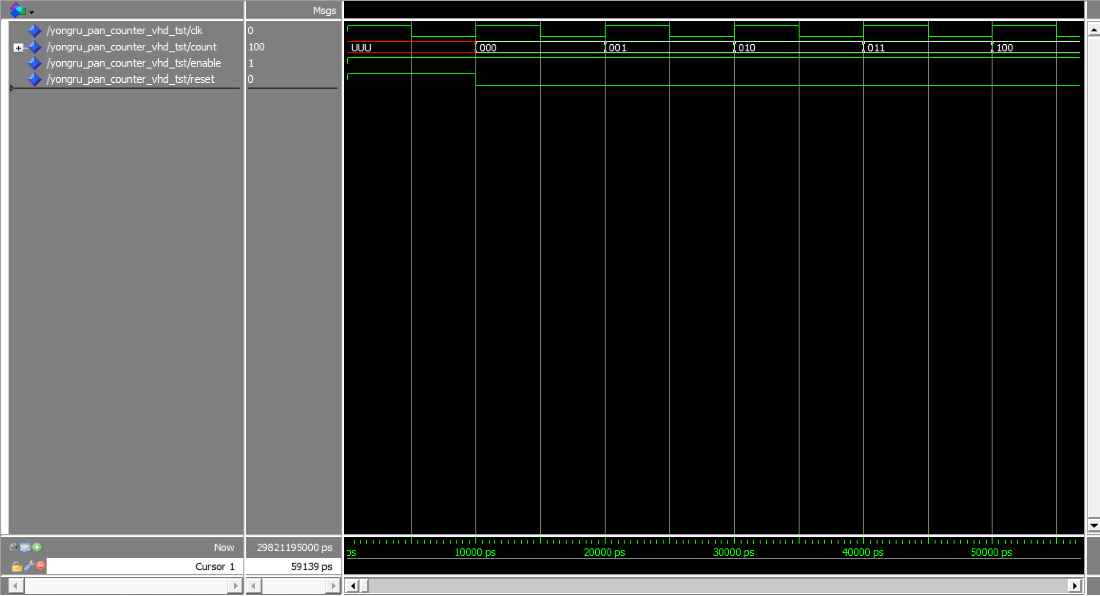
4. logic utilization 8, total pins 14

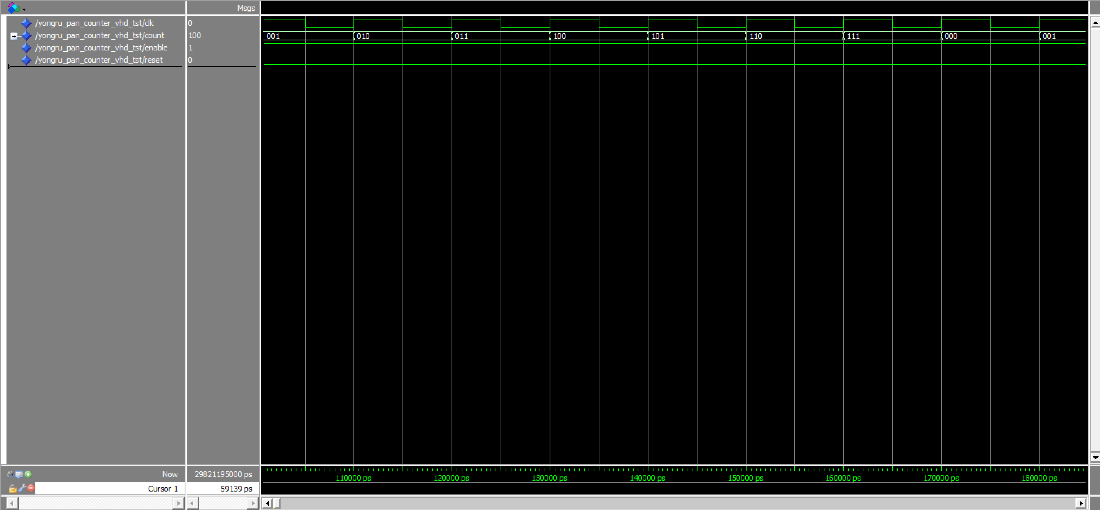
5.waveform for everything

1. JKFF

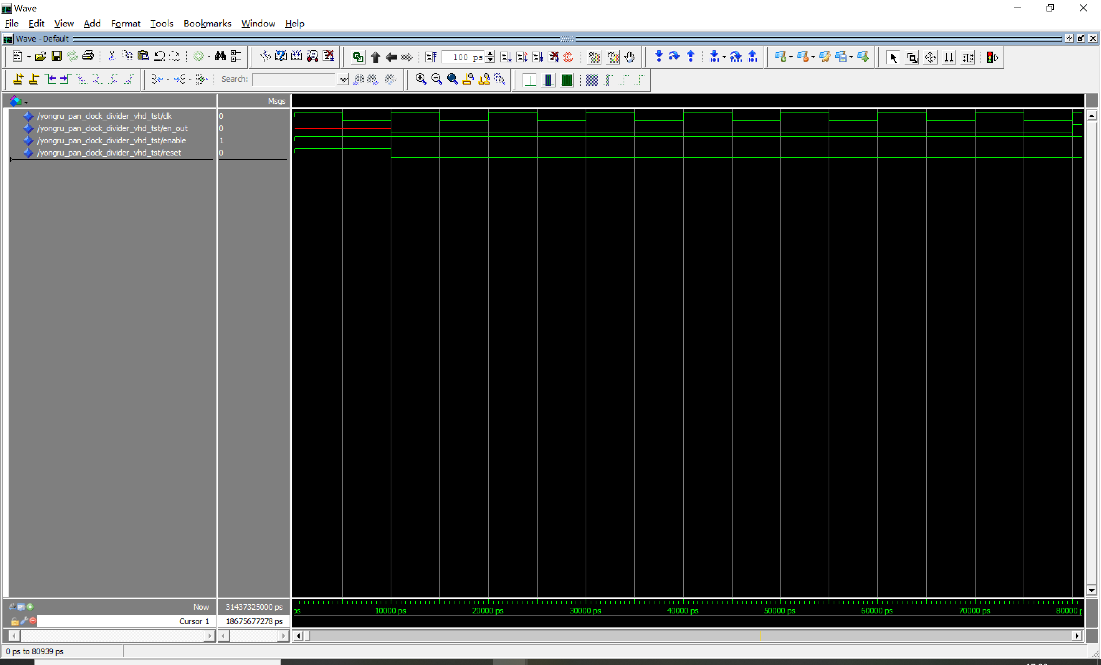


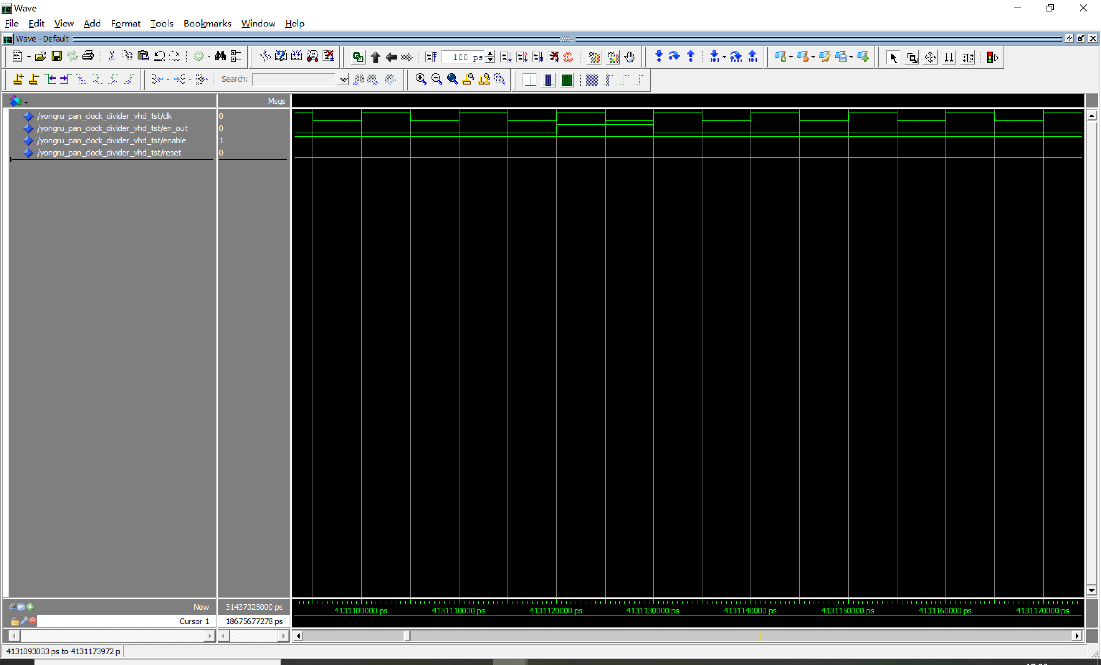
2. Counter



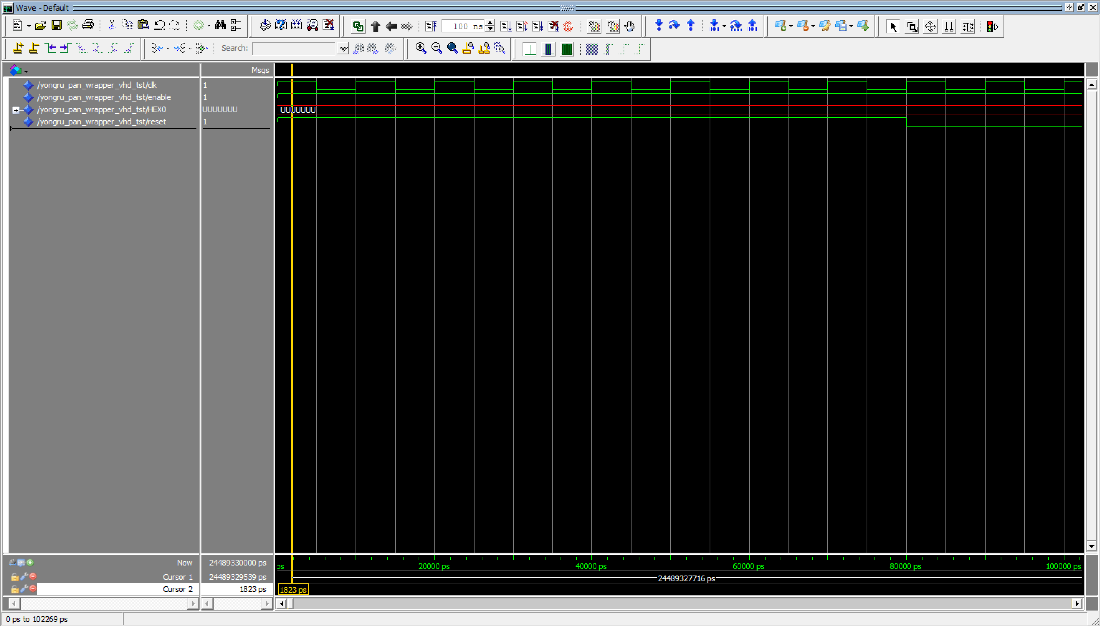


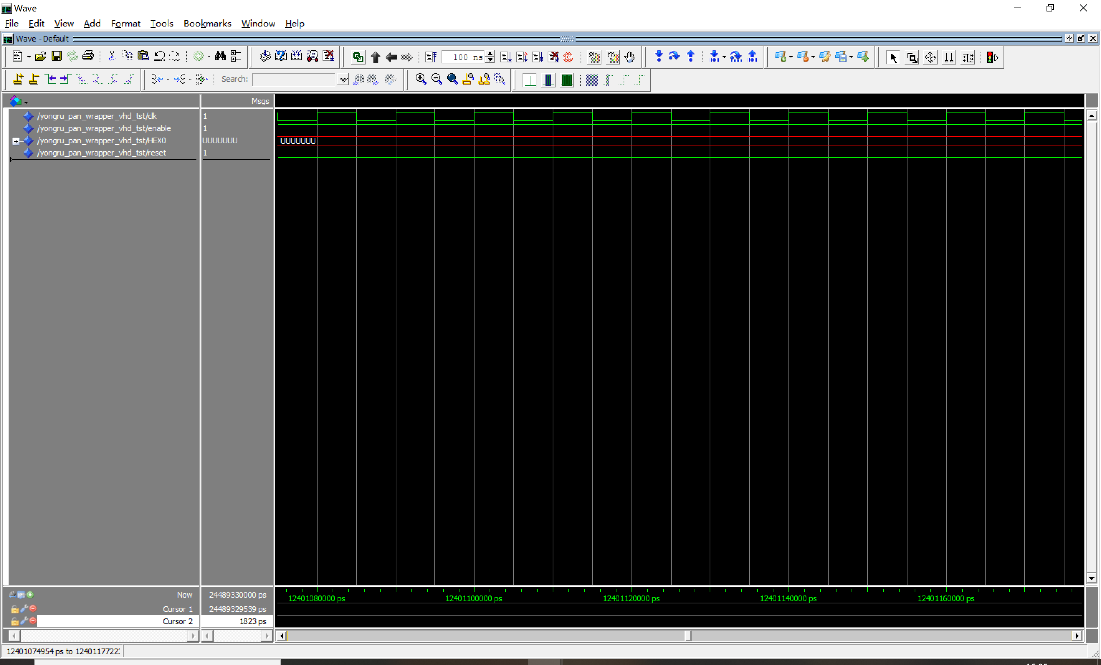
3. Clock divider



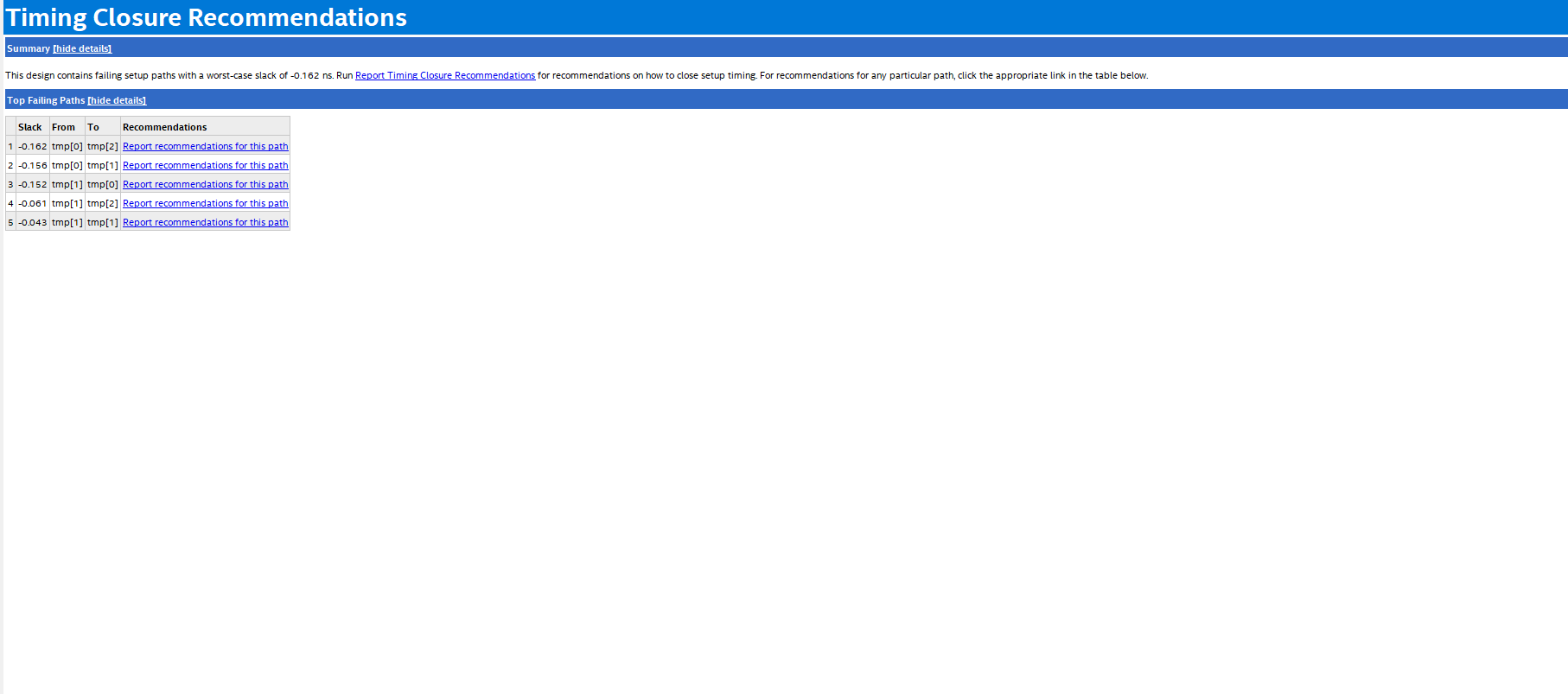


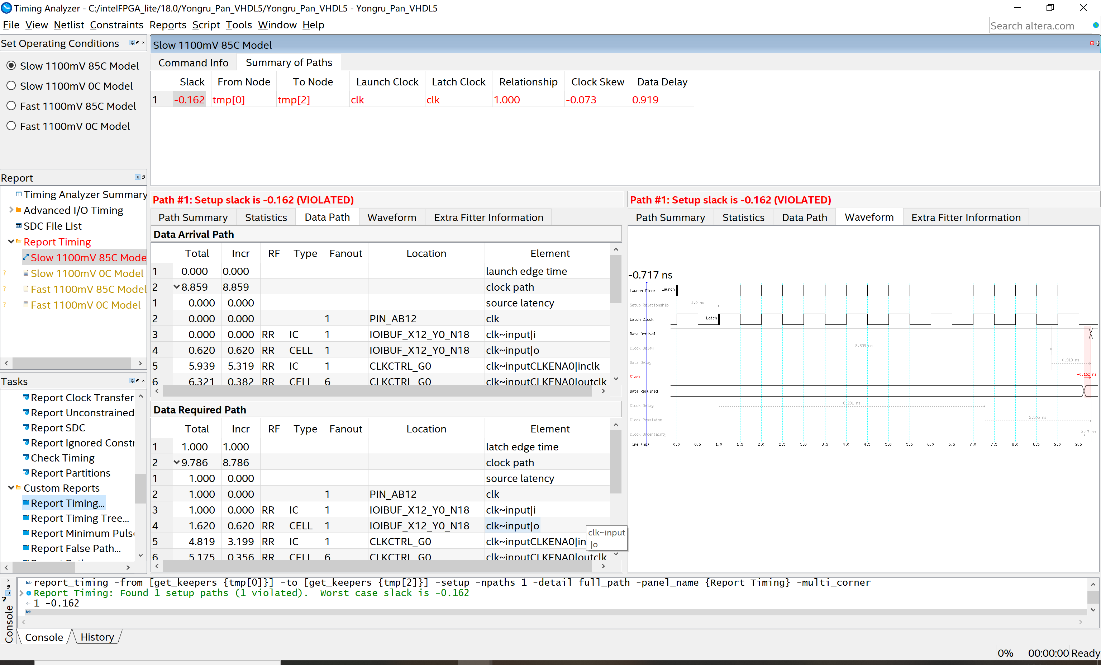
4. Wrapper





6. Critical path of counter





7. logic utilization N/A, total pins 6

**Conclusion**

All parts of experiments simulated successfully as required. The experiment has successfully describe a 4-bit comparator circuit in VHDL and has successfully done a demo and tested it on the Altera DE1-SoC board. A 3-bit up-counter and a clock-divider has also been successfully designed and simulated on Model Sim. The wrapper is created with up-counter and clock divider as component and has successfully assigned pin and have input simulation on ModelSim.